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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/772,750	02/04/2004	Koichi Yamada	P18129	5683

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EXAMINER	
GEIB, BENJAMIN P	

ART UNIT	PAPER NUMBER
2181	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/772,750	YAMADA ET AL.	
	Examiner	Art Unit	
	BENJAMIN P. GEIB	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 November 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

2. Claims 1-3, 5, 10, 12, 13, and 15-24 are rejected under 35 U.S.C. 102(a) as being anticipated by Sandri et al., U.S. Patent No. 7,428,732 (hereinafter Sandri).

3. As per claim 1, Sandri discloses a method comprising:

in a processor based system where a plurality of logical processors *[Fig. 1, components 101 and 102]* of a single physical processor *[device; Fig. 1, component 100]* share processor execution resources of the single physical processor *[column 4, lines 1-9]*, in response to a first logical processor in the plurality of processors being scheduled to enter an idle state due to lack of scheduling tasks *[when a logical processor lacks scheduling tasks, all of its reserved resources will be released; column 5, lines 25-28]*, making a processor execution resource previously reserved for the first logical processor available to any of the plurality of logical processors *[when the previously reserved resources are released, then they are available to other logical processors; column 5, lines 25-28]*.

4. As per claim 2, Sandri discloses further comprising reserving the processor execution resource for the first processor in response to the first processor being scheduled to execute a task *[column 4, lines 27-38]*.

5. As per claim 3, Sandri discloses wherein each of the plurality of processors is a logical processor of the processor based system *[column 4, lines 1-9]*.

6. As per claim 5, Sandri discloses wherein making the processor execution resource previously reserved for the first processor available to any of the plurality of processors further comprises releasing the processor execution resource into a common pool of processor execution resources *[See Fig. 1, Shared Resource; column 5, lines 25-28]*.

7. As per claim 10, Sandri teaches a processor comprising:

A single physical processor *[device; Fig. 1, component 100]* that implements a plurality of logical processors *[Fig. 1, components 101 and 102]]*; and logic to execute an instruction set which when executed by a first logical processor, cause the first logical processor to make a processor execution resource previously reserved for the first processor available to a second processor in the plurality of processors *[when the previously reserved resources are released, then they are available to other logical processors; column 5, lines 25-28]* in response to the first logical processor being scheduled to enter an idle state due to lack of scheduling tasks *[when a logical processor lacks scheduling tasks, all of its reserved resources will be released; column 5, lines 25-28]*.

8. As per claim 12, Sandri discloses wherein causing the first logical processor to make the processor execution resource previously reserved for the first logical processor available to a second logical processor further comprises releasing the processor execution resource into a common pool of processor execution resources accessible from the second logical processor *[]*.

9. As per claim 13, Sandri discloses wherein the processor execution resource previously reserved for the first logical processor further comprises the processor execution resource previously statically allocated to the first logical processor; and wherein releasing the processor execution resource into a common pool of processor execution resources further comprises de-allocating the processor execution resource *[See Fig. 1, Shared Resource; column 5, lines 25-28]*.

10. As per claims 15-19, Sandri discloses the limitations of the claims for similar reasoning to above rejections of claims 10-14. The difference between these two sets of claims is claims 15-19 are directed to a system, which Sandri discloses in column 10, line 39 - column 11, line 15. Claim 15 also has the added limitation of wherein the system comprises firmware to schedule the first logical processor to enter an idle state (column 4, lines 7-9) and a bus to interconnect the firmware and the processor (See Fig. 1, connection between access control software and device; column 4, lines 7-9).

11. As per claims 20-24, Sandri discloses the limitations of the claims for similar reasoning to above rejections of claims 1-5. The difference between these two sets of claims is claims 20-28 are directed to a machine accessible medium having stored thereon data which when accessed by a machine causes the machine to perform a method, which Sandri discloses in column 8, lines 49-57.

Claim Rejections - 35 USC § 103

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

13. Claims 4, 6-9, 11, 14, 25-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sandri.

14. As per claims 4 and 11, taking claim 4 as exemplary, Sandri discloses wherein the first processor being scheduled to enter an idle state. Sandri has not explicitly taught that the first processor executes a processor instruction requesting the first processor to enter an idle state. However, processor instructions requesting a processor to enter an idle state are conventional and well-known. At the time the invention was made, it would have been obvious to one of ordinary skill in the art to modify the invention of Sandri so that the first processor would execute a processor instruction requesting the first processor to enter an idle state. The motivation for doing so would have been to reduce power consumption.

15. As per claim 6, Sandri has taught the method of claim 2. Sandri has not explicitly taught wherein the first processor being scheduled to execute a task further comprises the first processor receiving a wake up signal. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to have modified Sandri so that the first processor would enter an idle state. It when then be necessary for proper processor operation to provide a wake up signal to allow the processor to later resume execution. The motivation for doing so would have been to reduce power consumption.

16. As per claim 7 and 14, taking claim 7 as exemplary, Sandri discloses wherein the processor execution resource is previously reserved for the first processor and wherein releasing the processor execution resource into a common pool of processor execution resources further comprises de-allocating the processor execution resource [See column 5, lines 25-28; execution resources are release after being reserved for a logical processor]. Sandri has not explicitly taught that the execution resource is statically

allocated to the first processor. However, static allocation of execution resources is conventional and well-known. At the time the invention was made, it would have been obvious to one of ordinary skill in the art to modify Sandri such that some of the execution resources are initially statically allocated to a particular logical processor. The motivation for doing so would have been to prevent the overhead and potential conflict of resource allocation at startup.

17. As per claim 8, Sandri discloses wherein the processor execution resource previously reserved for the first processor is locked by the first processor *[column 4, lines 27-39]*; and wherein releasing the processor execution resource into a common pool of processor execution resources further comprises the first processor unlocking the processor execution resource *[column 5, lines 25-34]*.

18. As per claim 9, Sandri teaches the method of claim 5. Sandri does not teach a translation lookaside buffer. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to have modified Sandri to include in the common pool of processor execution resources a translation lookaside buffer such that the processor execution resource is a translation cache entry from the translation lookaside buffer. A translation lookaside buffer is well known and commonly used in the art.

19. As per claims 25-28, Sandri teaches the limitations for the similar reasoning as for claims 6-9.

Response to Arguments

20. Applicant's arguments with respect to claims 1-28 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

21. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to BENJAMIN P. GEIB whose telephone number is (571)272-8628. The examiner can normally be reached on Mon-Fri 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Alford Kindred can be reached on (571) 272-4037. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Alford W. Kindred/
Supervisory Patent Examiner, Art Unit 2181

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